WHAT IS CLAIMED IS:

1. A method for receiving a plurality of frame programs, said method comprising:

generating a first interrupt at a first predetermined offset from a starting point of a first time division multiple access (TDMA) frame;

receiving a first frame program responsive to the first interrupt in a first memory region;

executing the frame program during the first TDMA frame;

generating a second interrupt at a second predetermined offset from a starting point of a second TDMA frame; and

receiving a second frame program responsive to the second interrupt in a second memory region.

2. The method of claim 1, further comprising:

generating a third interrupt at a third predetermined offset from a starting point of a third TDMA frame; and

receiving a third frame program responsive to the third interrupt in the first memory region.

3. The method of claim 1, wherein executing the first frame program further comprises:

determining a first starting address associated with the first memory region; and

executing an instruction stored in the starting address.

4. The method of claim 3, wherein determining the starting address associated with the first memory region further comprises:

examining the contents of a register bit, wherein the register bit stores a first indicator or a second indicator;

determining that the first starting address is a predetermined default address, wherein the register bit stores the first indicator; and

determining that the first starting address is a split address, wherein the register bit stores the second indicator.

5. The method of claim 4, further comprising:

determining the split address by examining a split address register, wherein the register bit stores the second indicator.

6. A system for receiving a plurality of frame programs, said system comprising:

an interrupt generator for generating a first interrupt at a first prédetermined offset from a starting point of a first time division multiple access (TDMA) frame and for generating a second interrupt at a second predetermined offset from a starting point of a second TDMA frame;

a first region of memory for receiving a first frame program responsive to the first interrupt, wherein the first region of memory forms a portion of a random access memory;

a microsequencer for executing the frame program during the first TDMA frame; and

a second region of memory for receiving a second frame program responsive to the second interrupt, wherein the second region of memory forms a portion of a random access memory.

7. The system of claim 6, wherein the

interrupt generator generates a third interrupt at a third predetermined offset from a starting point of a third TDMA frame; and

wherein the first memory region stores a third frame program, responsive to generation of the third interrupt.

8. The system of claim 6, further comprising:

control registers for determining a first starting address associated with the first memory region; and

wherein the microsequencer executes an instruction stored in the starting address.

9. The system of claim 8, wherein the control registers further comprise:

a register bit for storing a first indicator or a second indicator, wherein storing the first indicator indicates that the start address is a predetermined default address, and wherein storing the second indicator indicates that the start address is a memory split address.

10. The system of claim 9, wherein the control registers further comprise:

a memory split address register for storing the memory split address.

11. An apparatus for receiving a plurality of frame programs, said apparatus comprising:

a random access memory comprising:

a first memory region; and

a second memory region; and

a microsequencer connected to the random access memory, wherein the microsequencer executes a first frame program stored in the first memory region during a first TDMA frame and a second frame program stored in the second memory region during a second TDMA frame.

12. The apparatus of claim 11, wherein the microsequencer executes a third frame program stored in the first memory region during a third TDMA frame.

13. The apparatus of claim 11, further comprising:

control registers connected to the microsequencer, wherein the control registers comprise:

a register bit storing either a first indicator or a second indicator, wherein if the register bit stores the first indicator, the microsequencer executes instructions stored in the first memory region, and wherein if the register bit stores the second indicator, the microsequencer executes the instructions stored in the second memory region.

14. The apparatus of claim 13, wherein the control registers further comprise:

a memory split address register for storing a memory split address;

wherein the memory split address is the starting address of the second memory region; and

wherein a predetermined default address is the starting address of the first memory region.